ABSTRACT

A fractional-type phase-locked loop circuit, for synthesising an output signal multiplying a frequency of a reference signal by a selected fractional conversion factor, includes a frequency divider for generating a feedback signal dividing the frequency of the output signal by a frequency division factor selectable among at least two different integer-value division factors, and frequency divider control means for causing the frequency division factor to vary between the at least two integer-value division factors in a pre-defined number of cycles, thereby an average frequency division factor over said pre-defined number of cycles has a fractional value. Means are provided for compensating a phase error introduced by the frequency divider on the basis of a value indicative of the phase error obtained from said frequency divider control means. The phase-error compensation means includes rounding means, receiving an input binary code with a first number of binary digits, indicative of the phase error value, and providing an output binary code, with a second number of binary digits lower than the first number of digits, defining a rounded phase error value.